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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,652	09/26/2003	Frankie F. Roohparvar	400.067US05	8224

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EXAMINER	
NGUYEN, TAN	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,652	ROOHPARVAR, FRANKIE F.	
	Examiner	Art Unit	
	Tan T. Nguyen	2818	

-- The MAILING DATE f this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 5-8* is/are rejected.

7)☒ Claim(s) *3 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following action is in response to the amendment filed by Applicant on April 5, 2004.

2. Claims 1-8 are pending.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 5-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Tang et al. (U.S. Patent No. 6,172,915).

Tang et al. disclose in figure 1 an EEPROM memory device having an algorithmic state machine [34,34a] (column 4, line 10) coupled to a memory cell array [10] formed of a plurality of sector 0 through sector 7 corresponding to selectable blocks [12,14,16,18,20,22,24,26] respectively (column 3,lines 64 to column 4,line 1) via a word line decoder [28] and a column decoder [30] (column 4, line 5), an erase pulse generator [36] is coupled to the state machine 34] (column 4, lines 16-18). Tang et al. disclose an erased memory cell having a state "1" (column 4, lines 29-30). The sectors [12-26] in figure 1 would be considered as the claimed block or sub-blocks in claims 1, 6 and 8 of the present application. Tang et al. disclose in Figures 3a-3c an erase method in which a in block [310] of Figure 3a, a an erase-on signal is switched or turned ON only for sector that need to be erased, the erase-on signal is switched ON only for sectors that need to be erased and that have not passed completely an erase-

verify operation (column 5, lines 37-47). This block [310] would be considered as the step of selecting an addressable block of memory cell in claim 1 of the present application. In block [314] the first address such as address 0 of each sector with its erase-on signal turned ON will be set to the current address for those sectors (column 5, lines 64-67). Tang et al. disclose block [318] will check the current address for the sector 0 to determine if it is in the state "1" (erased state) (column 6, lines 14-16). This block [318] would be considered as the step identifying an address of a memory cell and performing an erase verification of the memory cell in the present application because Tang et al. disclose in the block [318] if any current address for sector 0 it is determined by the decision block [318] to be not in the state "1", only the location of this current address is stored in an address register so as to remember where in the sector 0 that the erase verifying operation failed (column 6, lines 30-37). Tang et al. further disclose if at any current address it is determined by the decision block [328] to be not in the state "1", then at block [34] an erase pulse from the erase pulse generator [36] will be issued to all the bytes in all the sectors having their erase-on signal not turned OFF as controlled by the state machine [34a]. Then the erase-verify operation will continue in the blocks [316] and [318] for the first sector having its erase-on signal turned ON beginning at the address that failed to erase verify prior to the issuance of the erase pulse (column 6 line 66 to column 7, line 7).

Regarding claim 2, Tang et al. disclose a separate address register is required for each sector so as to store the address where the erase-verify operation failed (column 7, lines 18-21).

Regarding claim 5, Tang et al. disclose in block [312] all bytes in the sectors having their erase-on signal turned ON are pre-programmed to a logic state "0" (column 5, lines 53-56) in addition to the other steps in the erase operation in Figures 3a-3c.

Regarding claims 6 and 8, the erase-on signal for each sector would be considered as the claimed erase indication register.

Regarding claim 7, Tang et al. disclose the state machine [34] in figure 1.

As to the limitation of the address of the memory cell is greater than a lowest address in the selected addressable block in claims 1, 6 and 8 of the present application, Tang et al. disclose the erase operation for each sector starts with the starting address would be address 0 of the sector and the last address would be the last address of the sector, and the first address of the sector with its erase-on signal turned ON will be set to be the current address for the sector (column 5, lines 61-67). As the erase operation is sequentially performed from the address 0 to the last of the sector, the current address is always greater than the lowest (address 0) of the sector.

5. Claims 3-4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Applicant's arguments with respect to claims 1-2 and 6-8 have been considered but are moot in view of the new ground(s) of rejection.

7. REMARKS

Applicants asserted Honda et al. showing a block register 42 hold information for block that have been selected to be erased, but not the block that have already been erased an require verification. Application also stated Honda et al. neither teach nor suggest Applicant's claimed method for performing an erase verification on a memory array. New reference to Tang et al. disclose an erase operation similar to Application's method wherein the address of the memory cells that failed the erase verify operation are stored and erase pulse and erase verification are only applied to the failed memory cells starting with the memory cells having their addresses stored in an address register.

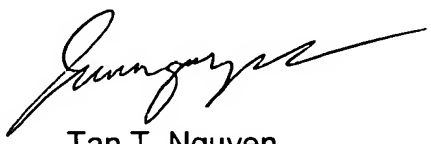
8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hung is cited to show a memory device having erase verify operation.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (703) 308-1298. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms, can be reached at (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tan T. Nguyen
Primary Examiner
Art Unit 2818
April 28, 2004